

CORELIS

USB-1149.1/1E

USB-1149.1/1E **High-Speed USB Port** **Boundary-Scan Controller**

User's Manual

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Chapter 1: Product Overview

Introduction

The USB-1149.1/1E High-Speed Boundary-Scan (JTAG) Controller is a member of the Corelis ScanExpress™ family of scan-based test, analysis, and diagnostic tools. The USB-1149.1/1E interfaces between a PC equipped with a USB2.0 port and any IEEE Standard 1149.1 compatible target. The USB-1149.1/1E is designed to control the operation of an IEEE Standard 1149.1 boundary-scan (JTAG) test access port (TAP) by generating the proper signals under software control to interface with the target device. It contains memory-behind-the-pin architecture and supports scan operations at continuous JTAG clock (TCK) speeds of up to 100 MHz.

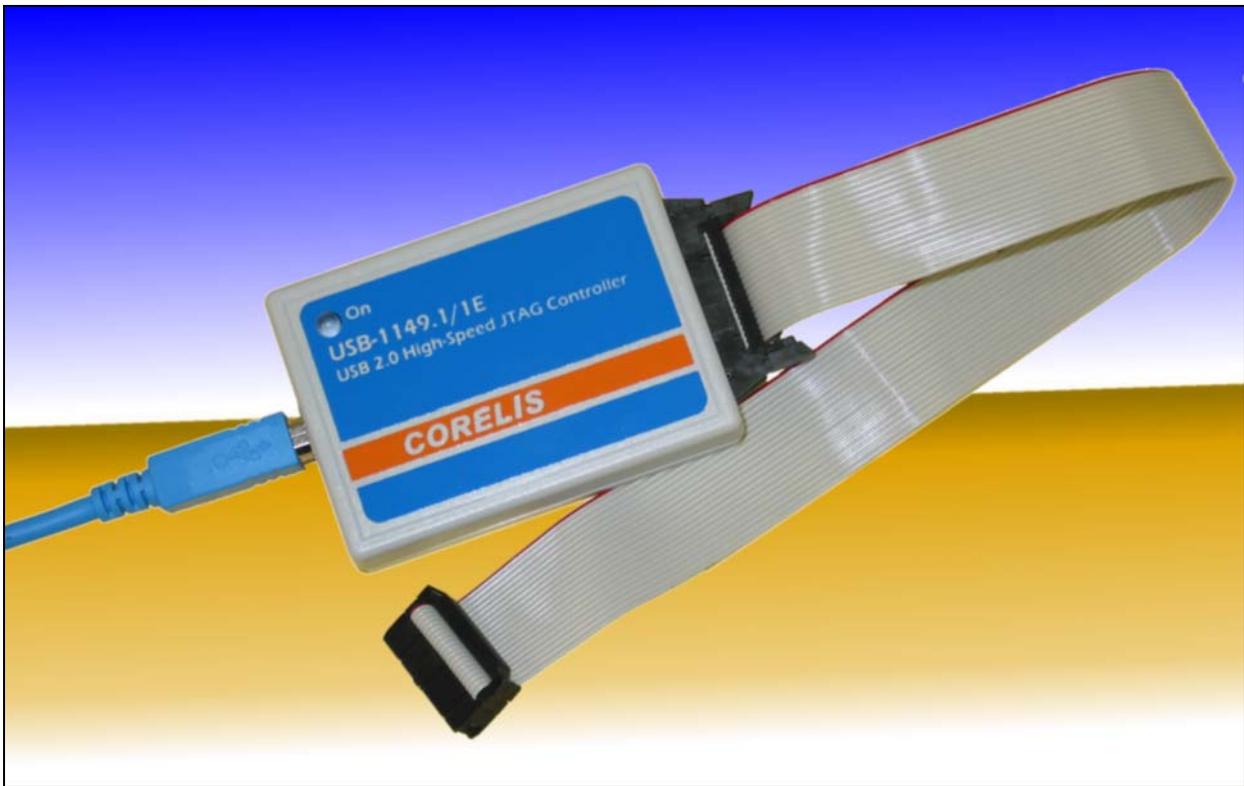


Figure 1-1. USB-1149.1/1E Boundary-scan Controller

The USB-1149.1/1E facilitates software-controlled boundary-scan operations per IEEE Standard 1149.1. It provides command access to the target's Test Access Port (TAP), accessing device internal registers and on-chip debugger, verifying PCB interconnects, performing functional testing, and debug without manual probing. The JTAG interface also provides access to internal device functions that are not accessible via external probing, enabling fault isolation within the device itself. The JTAG interface also enables programming target Flash and CPLD devices, as well as data download and uploading to and from the target memory devices.

What is IEEE Standard 1149.1?

The USB-1149.1/1E facilitates software-controlled boundary-scan operations per IEEE Standard 1149.1. It provides command access to the target's Test Access Port (TAP), accessing device internal registers and on-chip debugger, verifying PCB interconnects, performing functional testing, and debug without manual probing. The JTAG interface also provides access to internal device functions that are not accessible via external probing, enabling fault isolation within the device itself. The JTAG interface also enables programming target Flash and CPLD devices, as well as data download and uploading to and from the target memory devices.

The USB-1149.1/1E is often used to perform microprocessor emulation via the device JTAG port. It is used for firmware development providing single-step, break, and content update/visibility access.

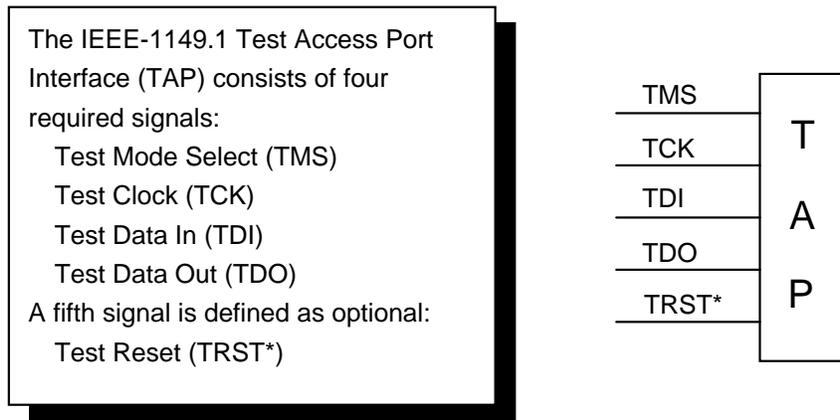


Figure 1-2. Minimal Test Access Port

Features of the USB-1149.1/1E

The Corelis USB-1149.1/1E is a sophisticated test controller that can access devices, boards or systems compliant with IEEE Standard 1149.1. The USB version 2.0 port compatible module supports a single JTAG boundary-scan chain (TAP). In addition, three general purpose, bi-directional discrete I/O signals can test or control non-boundary-scan areas of the unit under test (UUT). The discrettes can also assist in greatly expediting certain long scan activities, such as Flash programming. With its software-controlled voltage translating logic for all the above signals, the USB-1149.1/1E can test low voltage systems.

The USB-1149.1/1E contains several performance enhancing functional sections aimed at streamlining test vector throughput and emulator target download/upload transfers. Key functional elements include the TAP controller, and the memory resources that support it. The on-board memory provides scan data buffering and can at times store the entire scan data for maximum performance, real-time scan operations.

A test system operates the TAP controller and its associated memory through the host USB (2.0, with 1.1 backward compatibility) Port. The high data rate of the USB 2.0 Port is fully supported (up to 480 Mbit/sec.), regardless of actual test clock speeds. This latter TCK rate can operate up to 100 MHz depending on selected signal voltages and target conditions. The on-board memory elements further decouple the scan operations from the host software. A hardware state machine that contains status and control registers accessible through the USB Port directly controls all functions of the USB-1149.1/1E.

Hardware mechanisms enable optimal data flow between the USB port and the memory resources paced by the port and/or scanning rates underway, in both directions.

A programmable, time delay skew compensation mechanism supports the USB-1149.1/1E's high TCK clock rates. It accommodates the returned target scan stream delays due to signal travel time down and up the cable. It can also adjust for a target's internal TCK-to-TDO response delay.

Adjustable Voltage Levels

The software-programmable voltage level of the TAP interfaces and discrete I/O and can be set to any voltage between 1.25 V and 3.30 V in increments of about 0.05V.

Discrete Input/Output Signals

The USB-1149.1/1E operates three discrete input/output signals under software control. These attach to the target TAP connector. They are driven or sensed as directed by software, in coordination with the scanning operation. Each such signal can be configured independently as TTL output, open-collector (open-drain) output, or as input at the programmable voltage level. As open-collector drivers, they can readily tie to similar target signals without the need to alter its circuitry, yet still gain control of related functions, such as a Flash write signal.

As outputs, these discrettes are useful for providing control functions on the user target system such as general reset, power control, device write pulse, disable/enable and/or similar signals for non-boundary-scan target stimulus.

Conversely, as inputs, they enable host sensing of the target to pace scanning activity or related conditions (such as a Flash ready signal).

USB Port Interface

The USB-1149.1/1E operates under USB version 2.0 with backward compatibility to version 1.1 (excluding low speed). Speed adjustment is automatic per the standard. This host port also supplies the power to operate the USB-1149.1/1E. The hot plug-in/out feature of this standard is fully supported. The user simply plugs it into a PC USB socket, and it is auto-sensed and ready-to-scan.

For optimal performance, the user is recommended to utilize a host PC with a USB 2.0 port standard, given the considerably higher transfer rate.

Do not connect the USB-1149.1/1E to the host PC through a passive (un-powered) USB hub, as it may not provide the USB-1149.1/1E with adequate operating power from the host PC.

Programmable Clocks

The USB-1149.1/1E's programmable TCK output to the IEEE Standard 1149.1 compatible target system can be configured over a wide range of frequencies, using on-board clock generation circuitry. A programmable Phase Locked Loop (PLL) enables both a wide range and fine selection resolution. See Table 1-1 for the set of programmable values.

TCK range (MHz)	Rate Resolution (MHz)
15 to 100	1
1 to 15	0.5
0.05 to 1	0.05

Table 1-1. Programmable TCK Frequencies

Controllable Slew Rate

The USB-1149.1/1E supports slow or fast slew rate on the outputs.

Pin Protection

The USB-1149.1/1E features voltage detection circuitry to prevent the drivers from being damaged if the outputs are inadvertently shorted to power or ground.

USB-1149.1/1E Hardware Specifications

Physical

Mechanical Dimensions (box)	3.25 inches x 2.30 inches x 0.80 inches (+/- 0.10")
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Operating Environment

Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing

Storage Environment

Temperature	-40°C to 85°C
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Host Interface

USB Connector	Standard Type B Socket
Port Version	USB 2.0 port. Do not connect the USB-1149.1/1E to the host through a passive (un-powered) USB hub as it may not provide the USB-1149.1/1E with adequate operating power from the host PC.
Required Host CPU	Pentium III @ 1GHz or better
Required Operating System	Windows 2000, XP, Vista

Power Requirements

5V	Provided by the host USB 2.0 port in compliance with its requirements. Do not connect the USB-1149.1/1E to the host PC through a bus (passive/un-powered) powered USB hub as it may not provide adequate operating current. USB extender cables are not recommended.
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USB-1149.1/1E Electrical Specifications

JTAG TAP and Direct I2C/SPI Programming Interface

USB-1149.1/1E TAP Connector	20-pin (2x10) IDC header (0.100" x 0.100"), 3M part number: N3428-5302RB
USB-1149.1/1E TAP Connector Mating Connectors	20-pin (2x10) IDC receptacle (0.100" x 0.100"), 3M part number: 3421-6620
Minimum TCK Frequency	0.05 MHz
Maximum TCK Frequency	100 MHz
TCK Frequency Steps	0.05 MHz increments between 0.05 and 1 MHz 0.50 MHz increments between 1 and 15 MHz 1.0 MHz increments between 15 and 100 MHz
Maximum scanning data length	unlimited
Programmable Voltage (V _{adj}) Range	1.25V to 3.3V in 0.05V steps

Symbol	Test Conditions	Limit Min	Limit Max	Units
V _{IH}	V _{adj} ≥ 2.7 V	2	V _{adj} + 0.5	V
	V _{adj} < 2.7 V	0.65 × V _{adj}	V _{adj} + 0.5	V
V _{IL}	V _{adj} ≥ 2.7		0.8	V
	V _{adj} ≤ 2.0		0.35 × V _{adj}	V
V _{OH}	I _{OH} = -12 mA	V _{adj} - 0.5		V
V _{OL}	I _{OL} = 12 mA		0.4	V

Table 1-2. USB-1149.1/1E DC and Switching Characteristics

USB-1149.1/1E Indicator LED

When the USB cable is plugged in, the blue LED on top of the USB-1149.1/1E will turn on to indicate that the unit is receiving power from the computer.

Chapter 2: USB-1149.1/1E Installation

Installing the ScanExpress software and the USB-1149.1/1E hardware

The USB-1149.1/1E product consists of the following components:

- USB-1149.1/1E JTAG Controller Hardware
- USB-1149.1/1E User's Manual
- 6' USB 2.0 Cable
- 20-pin to 10-pin TAP Adapter Cable, Corelis P/N 15310-2
- 20-pin to 16-pin TAP Adapter Cable, Corelis P/N 15311-2
- 20-pin to 20-pin TAP Adapter Cable, Corelis P/N 15312-2

Please ensure that all materials listed are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, contact Corelis at the number shown on the title page immediately.

The following optional target interface cables are also available from Corelis:

- 20-pin to 14-pin EJTAG TAP Adapter Cable, Corelis P/N 15425
- 20-pin to 20-pin ARM TAP Adapter Cable, Corelis P/N 15432
- 20-pin to 15-pin ARC TAP Adapter Cable, Corelis P/N 15436
- 20-pin to 16-pin PowerPC TAP Adapter Cable, Corelis P/N 15433
- 20-pin to 16-pin PowerPC TAP Adapter Cable (Special Cable with Vsense for IBM Emulation), Corelis P/N 15442

Software Must Be Installed First!

The installation procedure requires the use of software that contains the driver for the USB-1149.1/1E module. Obtain the ScanExpress CD-ROM (or any other Corelis application that supports the USB-1149.1/1E module) in order to proceed with installation. Install the ScanExpress Application Software before installing the USB-1149.1/1E controller. The USB-1149.1/1E controller is a hot-pluggable USB device, and its drivers are installed with the ScanExpress Application Software. Windows will automatically recognize and configure the USB-1149.1/1E the first time it is detected in your system.

WARNING !

You **MUST** install the software first – before installing the unit. **Do not install the USB-1149.1/4E unit until you have successfully installed the application software** (ScanExpress, CodeRunner, etc.). Installing the software provides the hot-plug USB driver for the unit so that the operating system is able to properly detect and configure the unit. Installing the unit before the software may result in improper unit configuration and operation.

In the event that you installed the USB-1149.1/1E controller before installing the software, unplug the module, **cancel** the **Add/Remove Hardware Wizard** (that will automatically show up) and install the ScanExpress application from the CD. The next time you start the PC and plug in the USB-1149.1/1E, Windows will automatically recognize and configure the USB-1149.1/1E.

USB-1149.1/1E Hardware Installation

To install the USB-1149.1/1E on a host PC, follow the installation steps below. Note that you must install the application CD first and only then plug in the USB-1149.1/1E controller into an available USB port on the host PC. When Windows detects the controller, it will automatically start the **Found New Hardware Wizard** to guide the user through the driver installation process. The following section describes this process in detail under Windows XP with Service Pack 2. Note that the procedure may differ slightly depending on the version of windows.

Installation Steps:

1. Install the application software, such as ScanExpress Runner, from the CD on your computer.
2. Plug the USB cable of the USB-1149.1/1E module into an available USB mating connector on your PC.
3. The **Found New Hardware Wizard** dialog box will automatically start as shown below in Figure 2-1.
4. Select “**No, not this time**” as shown below and click on the **Next** button.



Figure 2-1. Found New Hardware Wizard (WinXP)

5. The following dialog box shown in Figure 2-2 will pop up. Select “**Install the software automatically (Recommended)**” and click on the **Next** button.

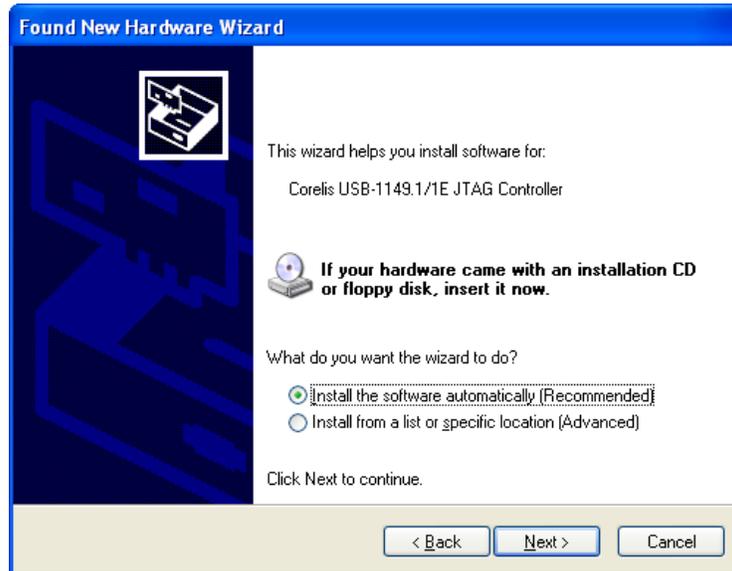


Figure 2-2. Found New Hardware Wizard (WinXP)

6. Under Windows XP, a warning dialog box will pop up indicating that the device driver has not passed Windows logo testing as shown in Figure 2-3. You can safely ignore the warning and continue the installation process by pressing the **Continue Anyway** button.



Figure 2-3. Windows Logo Warning Dialog (WinXP)

7. After the necessary files are copied to the system, the following dialog box, Figure 2-4, will pop up indicating that the device driver is successfully installed.

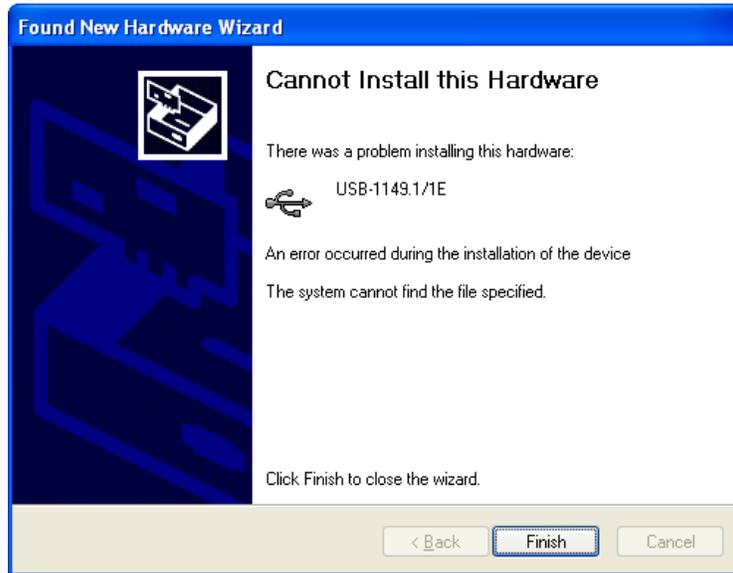


Figure 2-4. Installation Successfully Completed (WinXP)

8. Click on the **Finish** button to close the dialog box.

9. The installation of the device drivers is now completed. Verify that the USB-1149.1/1E was correctly installed by checking for its entry in the **Windows Device Manager**. To run the Device Manager, right mouse click on the **My Computer** icon and then select **Properties**. Choose the **Hardware** tab and click on the **Device Manager** button. Corelis **USB-1149.1/1E JTAG Controller** should be listed in the **Universal Serial Bus controller** section as shown in **Figure 2-5**.

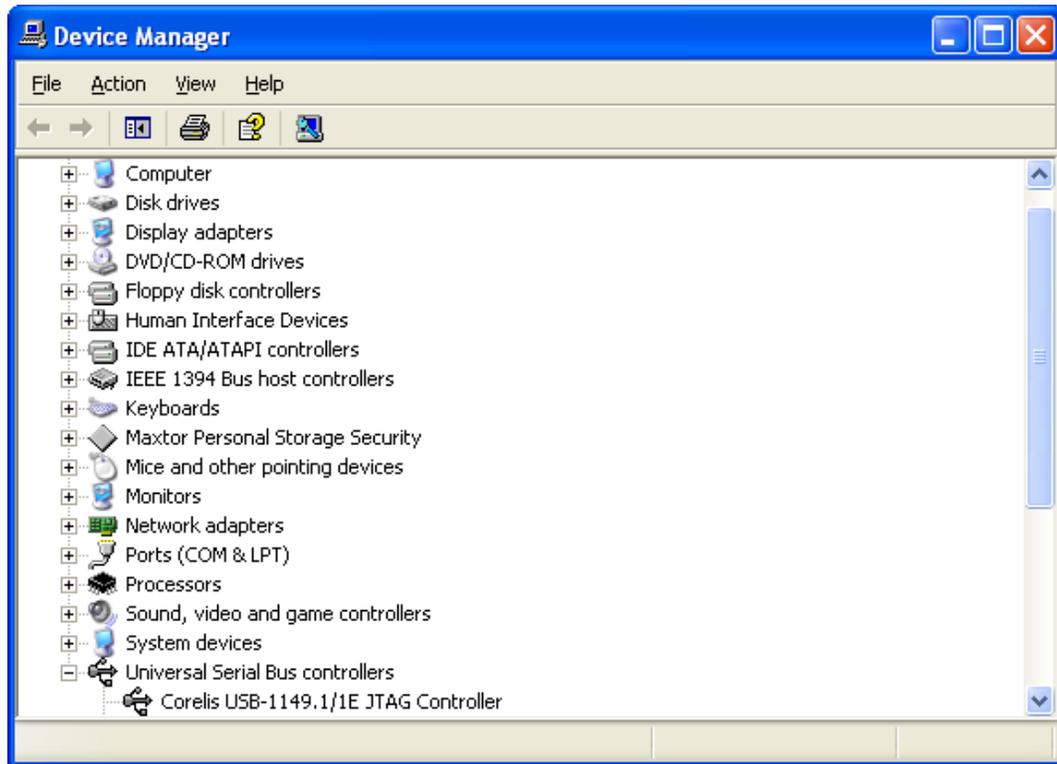


Figure 2-5. Windows Device Manager (WinXP)

Congratulations! You have now successfully installed the USB-1149.1/1E drivers on your computer and it is ready to be used. We suggest that you preserve the original packing material for the future shipment or storage of the USB-1149.1/1E.

Chapter 3: Connecting to the Target

Connecting to the Target

The connection to the target board/system is through the TAP connector on the front of the USB-1149.1/1E. Figure 3-1 shows the front view of the USB-1149.1/1E box, including the TAP connector pin numbering.



Figure 3-1. USB-1149.1/1E 20-pin TAP Connectors

To connect the TAP cables to the target (UUT), follow these steps in the order listed:

1. Verify that the target power is OFF.
2. Plug the TAP cable connector to the mating target header.
3. Now you can turn the target power ON.

ALERT !

Make sure your target board is connected to GROUND prior to powering up the target board. This assures that the target power return flows through its power supply return (GND) signal and not through the ground wire of the USB cable. Otherwise, with a 'floating' target if the user hot-plugs the target power cable from its external supply (such as a 'brick' type power supply) there is no guarantee that the ground will make contact with the target first, before the power does. In such case, it is possible to momentarily engage the voltage pin of the target power supply connector prior to engaging the ground (return) pin. During such action all target current will momentarily flow through the USB cable to ground with the resulting transients possibly resetting the USB-1149.1/1E unit.

Appendix A contains general recommendations for implementing compatible target TAP connector(s). Following these recommendations makes the connection to the target easy and straightforward.

To accommodate target boards with TAP connectors other than this standard, Corelis offers short, custom adapter cables for connectors such as the Altera ByteBlaster, the Xilinx 9-pin header, the Lattice TAP connector or the TI 14-pin DSP connector.

Connecting the TAP Signals

The USB-1149.1/1E contains a 20-pin TAP connector. The following table enumerates the pinout for the USB-1149.1/1E TAP connector.

Pin	Signal Name	Signal Description
1	TRST*	Test Reset (Input to the UUT)
2	GND	
3	TDI	Test Data In (Input to the UUT)
4	GND	
5	TDO	Test Data Out (Output from the UUT)
6	GND	
7	TMS	Test Mode Select (Input to the UUT)
8	GND	
9	TCK	Test Clock (Input to the UUT)
10	GND	
11	Write_Strobe* / SPI_CS2* / GPIO1	Discrete Output (Input to the UUT)
12	GND	
13	SPI_SCK / GPIO2	Discrete Output (Input to the UUT)
14	Reserved	[NOTE: may optionally be connected to GND]
15	Ready_Busy* / SPI_SDO (MISO) / GPIO3	Discrete Output (Input to the UUT)
16	SPI_SDI (MOSI)	Discrete Output (Input to the UUT) [NOTE: connect to GND if not used]
17	GPIO4	Discrete Output (Input to the UUT)
18	I2C_SCL	Discrete Output (Input to the UUT) [NOTE: connect to GND if not used]
19	GPIO5	Discrete Output (Input to the UUT)
20	SPI_CS1* / I2C_SDA	Discrete Output (Input to the UUT) [NOTE: connect to GND if not used]

Table 3-1. USB-1149.1/1E 20-pin Target Connector Pin Assignment

TAP Adapter Cable Pinouts

The following tables enumerate the pinout of the TAP connector for each of the USB-1149.1/1E TAP adapter cables.

UUT Pin	Signal Name	Signal Description
1	Not connected	
2	Not connected	
3	TRST*	Test Reset (Input to the UUT)
4	GND	
5	TDI	Test Data In (Input to the UUT)
6	GND	
7	TMS	Test Mode Select (Input to the UUT)
8	GND	
9	TCK	Test Clock (Input to the UUT)
10	GND	
11	Not connected	
12	GND	
13	TDO	Test Data Out (Output from the UUT)
14	GND	
15	SRST*	Target System Reset (Input to the UUT)
16	GND	
17	DISCR2	
18	GND	
19	DISCR0	
20	GND	

Table 3-2. ARM TAP Adapter Cable Pinout [P/N 15432 REV A]

UUT Pin	Signal Name	Signal Description
1	TDO	Test Data Out (Output from the UUT)
2	GND	
3	TDI	Test Data In (Input to the UUT)
4	TRST*	Test Reset (Input to the UUT)
5	Not connected	
6	Not connected	Target reference voltage
7	TCK	Test Clock (Input to the UUT)
8	Not connected	
9	TMS	Test Mode Select (Input to the UUT)
10	Not connected	
11	SRESET*	Soft Reset (Input to the UUT)
12	GND	
13	HRESET*	Hard Reset (Input to the UUT)
14	Not connected	
15	CHECKSTOP	Checkstop (Output from the UUT)
16	GND	

Table 3-3. PowerPC TAP Adapter Cable Pinout [P/N 15433 REV A]

UUT Pin	Signal Name	Signal Description
1	TDO	Test Data Out (Output from the UUT)
2	Not connected	[NOTE: may optionally be connected to GND]
3	TDI	Test Data In (Input to the UUT)
4	TRST*	Test Reset (Input to the UUT)
5	Not connected	
6	VSENSE	Target reference voltage
7	TCK	Test Clock (Input to the UUT)
8	Not connected	
9	TMS	Test Mode Select (Input to the UUT)
10	Not connected	
11	SRESET*	Soft Reset (Input to the UUT)
12	Not connected	[NOTE: may optionally be connected to GND]
13	HRESET*	Hard Reset (Input to the UUT)
14	Not connected	
15	CHECKSTOP	Checkstop (Output from the UUT)
16	GND	

Table 3-4. PowerPC TAP Adapter Cable (with Vsense) Pinout [P/N 15442 REV A]

Chapter 4: Using the USB-1149.1/1E with the ScanExpress Tools

Hardware Setup

You must configure the USB-1149.1/1E controller in a ScanExpress application before the application can use it. This chapter uses ScanExpress Runner as an example to illustrate the initial configuration process.

Using the USB-1149.1/1E with the ScanExpress Tools

The USB-1149.1/1E unit is compatible with ScanExpress Runner, ScanExpress Debugger and ScanExpress Programmer. The following steps are provided for ScanExpress Runner. Selecting the module in ScanExpress Debugger or ScanExpress Programmer is done in a similar fashion.

1. Make sure that USB-1149.1/1E controller is plugged in to your PC. Wait 3 to 5 seconds before starting any ScanExpress Applications if you just plugged in the controller.
2. Invoke the ScanExpress Runner application.
3. Click the **Setup** menu item and then select the **Controller** entry to display the Controller Configuration screen shown in Figure 4-1.

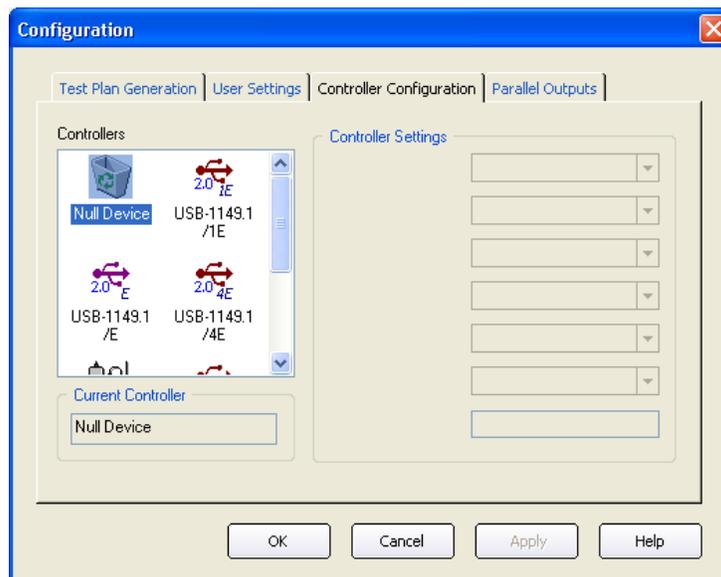


Figure 4-1. Controller Configuration Screen

4. Select the USB-1149.1/1E controller from the icons on the left. Adjust the controller settings to the desired values.
5. After you have made your selections, click on the Apply button to test and save the settings. When the program saves the settings successfully, it displays the controller in the Current Controller box. If ScanExpress Runner cannot find the controller, it displays an error dialog.
6. Once ScanExpress Runner finds the USB-1149.1/1E controller, it displays a screen similar to Figure 4-2.

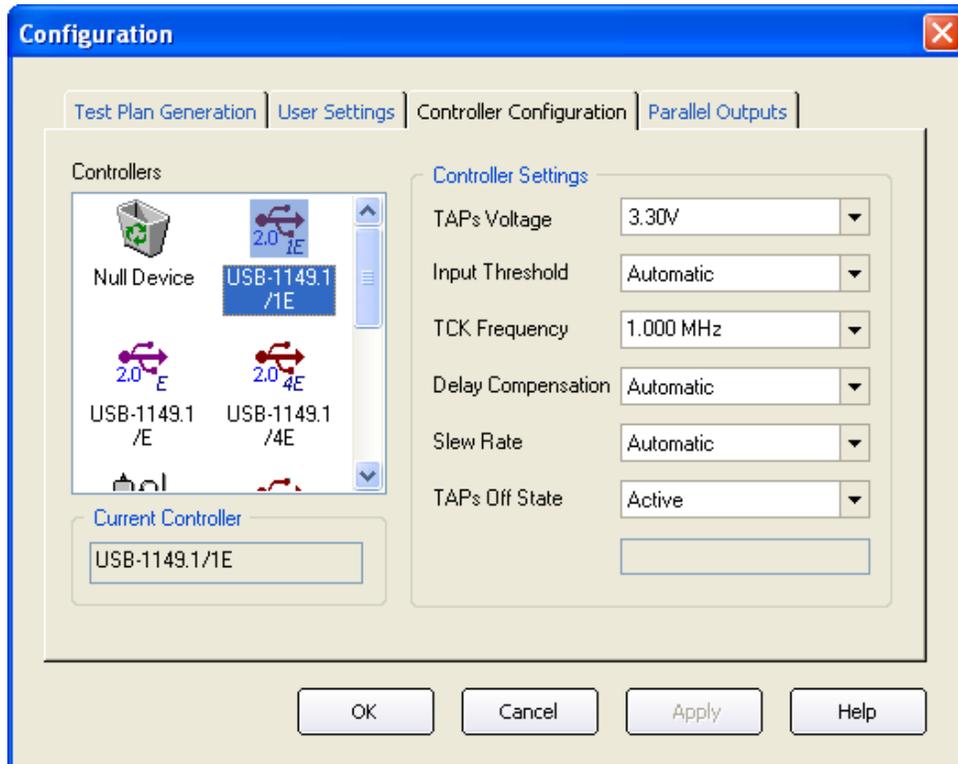


Figure 4-2. USB-1149.1/1E Setup Screen

Chapter 5: Third Party Application Interface

ScanExpress Runner provides a general purpose, third-party application interface that includes specifying the correct controller and settings. This section clarifies the requirements related to the USB-1149.1/1E unit. Refer to the ScanExpress Runner manual for further information.

Using the USB-1149.1/1E with the ScanExpress Runner Command-line

You can invoke ScanExpress Runner with special command line parameters to execute a Test Step file, provide test results and diagnostic messages in a log file (if you have the ScanExpress Runner ADO), and then terminate. The following table shows the controller identifiers and associated parameters. Consult the ScanExpress Runner User's Manual for more detail.

The USB-1149.1/1E controller uses 6 parameters. The parameters are described in the table below.

Controller keyword: **USB-1149.1/1E**

Position	Parameter	Value	Setting
1	TAPs Voltage	1	1.25 V
		2	1.30 V
	 (0.05 volts per step)
		41	3.25 V
		42	3.30 V
2	Input Threshold	1	Automatic
		2	0.50 V
		3	0.55 V
	 (0.05 volts per step)
		31	1.95 V
		32	2.00 V

Table 5-1. USB-1149.1/1E Controller Parameters

Position	Parameter	Value	Setting
3	Clock Frequency	1	100 MHz
	 (1 MHz increment)
		86	15 MHz
		87	14.5 MHz
	 (0.5 MHz increment)
		114	1 MHz
		115	0.950 MHz
	 (0.05 MHz increment)
4	Delay Compensation	133	0.050 MHz
		1	Automatic
		2	No Delay
		3	0.5 Clock Delay
		4	1.0 Clock Delay
		5	1.5 Clock Delay
		6	2.0 Clock Delay
		7	2.5 Clock Delay
5	Slew Rate	8	3.0 Clock Delay
		1	Automatic
		2	Slow slew rate
6	TAPs Off State	3	Normal slew rate
		1	Active (JTAG signals are driven when tests are not running)
		2	Tri-State

Table 5-1. USB-1149.1/1E Controller Parameters (continued)

Example:

To select a USB-1149.1/1E controller card with TAP voltage of 3.30 V, automatic threshold, TCK frequency of 1 MHz, automatic slew rate, automatic delay compensation, tri-state the JTAG signals (when test is finished), use the following “controller specification” string:

```
USB-1149.1/1E,42,1,114,1,1,2,
```

Appendix A: Recommended Target Connectors

10-pin TAP Connector

The Boundary-Scan TAP is a well defined IEEE-1149.1-compatible electrical interface between boundary-scan test equipment and the boundary-scan compatible devices in the user's target board. Boundary-scan based test equipment, such as the Corelis ScanExpress family of products, utilize a single TAP to interface to the UUT. This section explains how to implement a TAP connector that is compatible with most standard test equipment.

The TAP contains 5 signals: TCK, TMS, TDO, TDI and optionally TRST*. It also contains ground signal(s). Corelis recommends the standard TAP connector shown in Figure A-1, which is widely regarded as the industry standard. Note that each signal is terminated with a resistor (discussed below) in order to improve noise immunity.

The connector on the user's target should have a standard flat cable compatible pinout to match the TAP connector described in Table A-1. Figure A-1 shows the top view of the basic target 10-pin connector header (0.100 × 0.100 in. spacing):

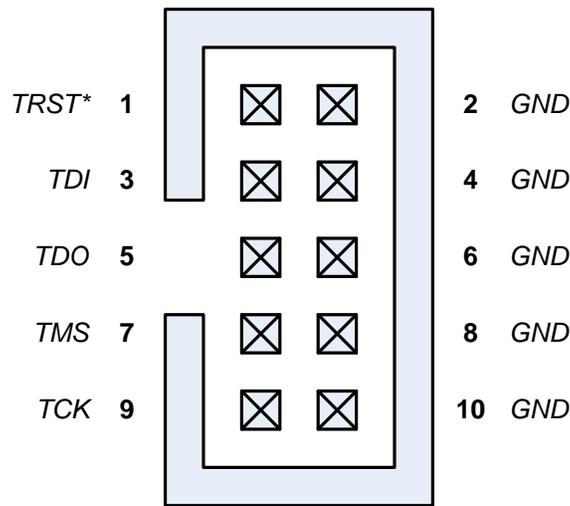


Figure A-1. Standard TAP connector (top view)

Table A-1 describes the 10-pin TAP connector signals and Corelis recommended values of terminating resistors:

Pin	Signal	Direction	Termination
1	TRST*	Input to the UUT	1K pull-up (or 1.5K pull-down)
2	GND		
3	TDI	Input to the UUT	1K pull-up
4	GND		
5	TDO	Output of the UUT	33 ohm series
6	GND		
7	TMS	Input to the UUT	1K pull-up
8	GND		
9	TCK	Input to the UUT	1K pull-up
10	GND		

Note: Some target boards may require a pull-down resistor on the TRST* signal to assure normal device operations when not in boundary-scan test mode.

Table A-1. Signal Description and Termination

Table A-2 summarizes the specifications for the 10-pin TAP connector. Equivalent connectors are available from other manufacturers.

Reference	Description	Manufacturer	Part Number
10-Pin Target TAP	Straight header, 10-pin, 4 wall, with center notch	3M	3473-6610

Table A-2. Standard 10-Pin TAP Connector

Figure A-2 shows a typical schematic of the target TAP connector with the recommended termination resistors. The 1K pull-up resistors should connect to the target Vcc supply corresponding to the interface voltage (programmable on the USB-1149.1/1E from 1.25 to 3.3 V). Recommended resistor values are +/- 5%.

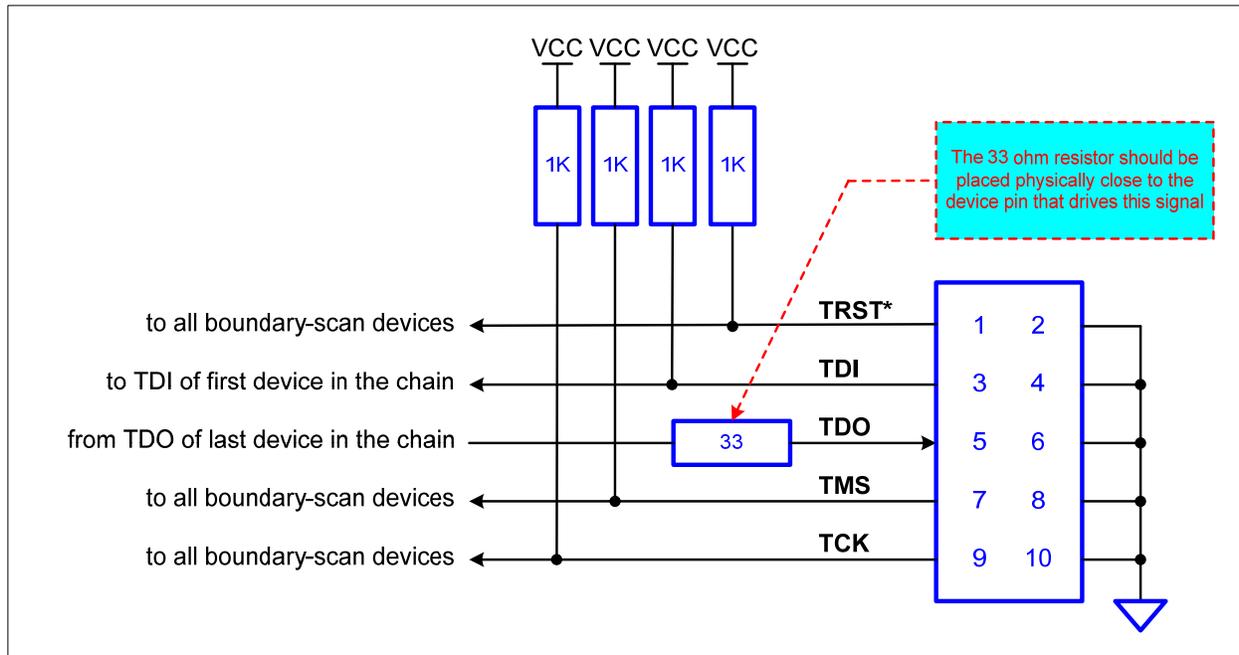


Figure A-2. 10-pin TAP Connector Schematic

16-pin TAP Connector

To build in support for in-circuit programming of flash or microprocessor devices, Corelis recommends including supplemental control signals in the TAP interface. The ScanExpress Programmer can use a 16-pin TAP, similar to Figure A-3, to improve programming time. This interface adds Write_Strobe*, Ready/Busy*, and ground signals to the standard 5-signal interface. Terminating resistors (see Table) can improve signal quality.

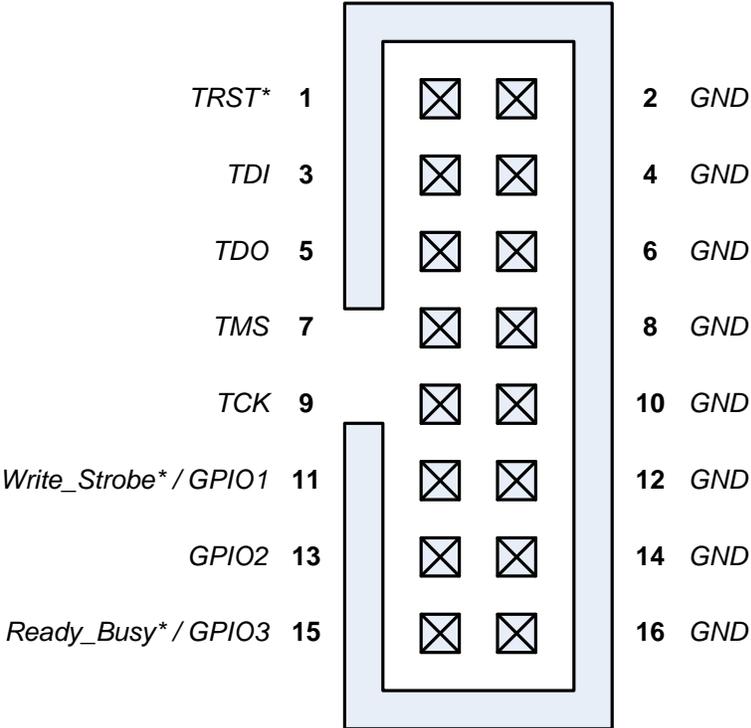


Figure A-3. Boundary-scan Flash Programming 16-Pin TAP Connector (top view)

Corelis’ Flash Programming software supports the external signals Write_Strobe* and Ready/Busy*, in addition to the standard but slower scanned out/in signals approach.

The Write_Strobe* signal is active low and should be pulled up with a 1K resistor on the target board. It needs to be logically ORed with the flash Write-Enable (WE*) signal so that either the flash Write-Enable (WE*) signal or the external Write_Strobe* going low will assert the flash WE* input.

The active low Ready/Busy* signal is typically an open-collector/open-drain signal that ties directly to the same signal(s) on the Flash device(s). This enables multiple devices to drive it toward the USB-1149.1/1E.

Table A-3 summarizes the specifications for a 16-pin TAP connector without latch ejectors. Equivalent connectors are available from other manufacturers.

Reference	Description	Manufacturer	Part Number
Flash TAP	Straight header, 16-pin, 4 wall, with center notch	3M	2516-6002UG

Table A-3. Flash Programming TAP 16-Pin Connector

Table A-4 describes the signals and Corelis recommended values of terminating resistors:

Pin	Signal	Direction	Termination
1	TRST*	Input to the UUT	1K pull-up (or 1.5K pull-down)
2	GND		
3	TDI	Input to the UUT	1K pull-up
4	GND		
5	TDO	Output from UUT	33 ohm series
6	GND		
7	TMS	Input to the UUT	1K pull-up
8	GND		
9	TCK	Input to the UUT	1K pull-up
10	GND		
11	Write_Strobe*	Input to the UUT	1K pull-up
12	GND		
13	GPIO2		
14	GND		
15	Ready/Busy*	Output from UUT	1K pull-up
16	GND		

Note: Some target boards may require a pull-down resistor on the TRST* signal to assure normal device operations when not in boundary-scan test mode

Note: The target TDI signal is driven by the TDO signal of the boundary-scan controller

Note: The target TDO signal drives the boundary scan controller's TDI signal

Table A-4. 16-pin Connector Signal Description and Termination

Figure A-4 shows a typical schematic of the target TAP connector with termination resistors. The 1K pull-up resistors should connect to the target Vcc supply corresponding to the interface voltage (programmable on the USB-1149.1/1E from 1.25 to 3.3 V). Recommended resistor values are +/- 5%.

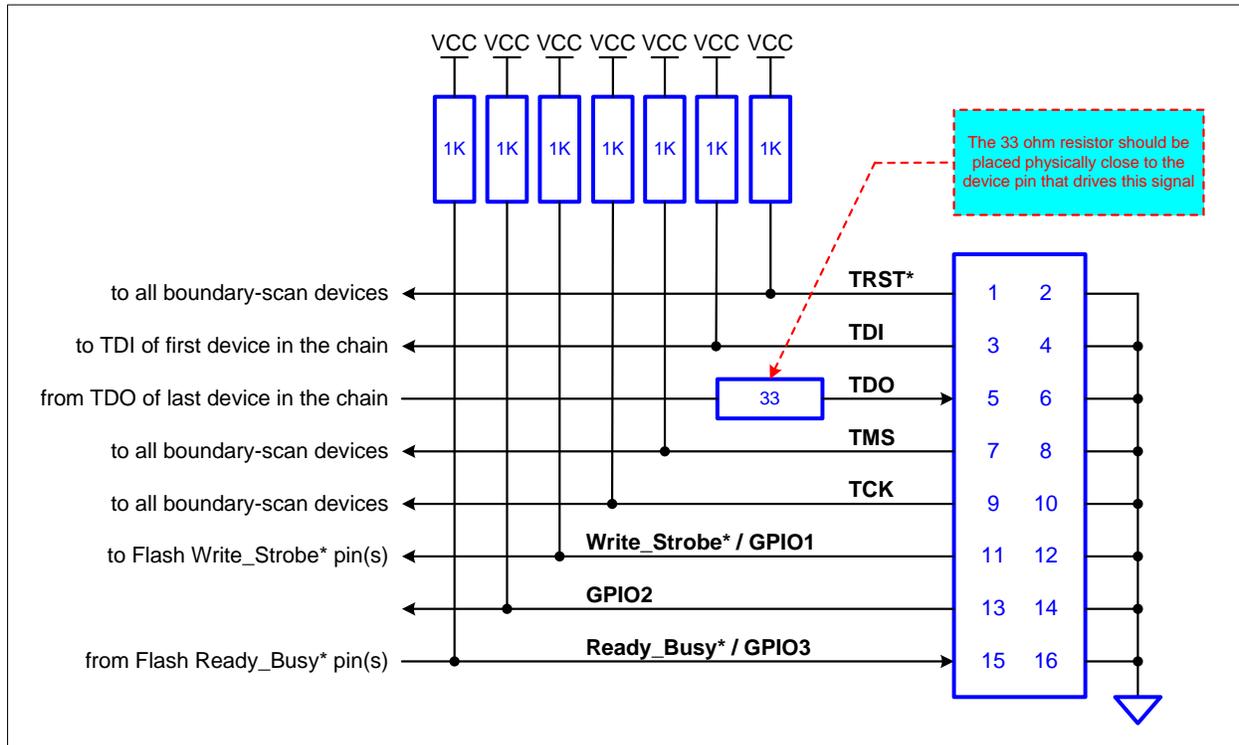


Figure A-4. 16-pin Flash Programming TAP Connector Schematics

20-pin TAP Connector

To build in support for in-circuit programming of flash or microprocessor devices, Corelis recommends including supplemental control signals in the TAP interface. The ScanExpress Programmer can use a 20-pin TAP, similar to Figure A-5, to improve programming time. This interface adds Write_Strobe*, Ready/Busy*, and ground signals to the standard 5-signal interface. Terminating resistors (see Table) can improve signal quality.

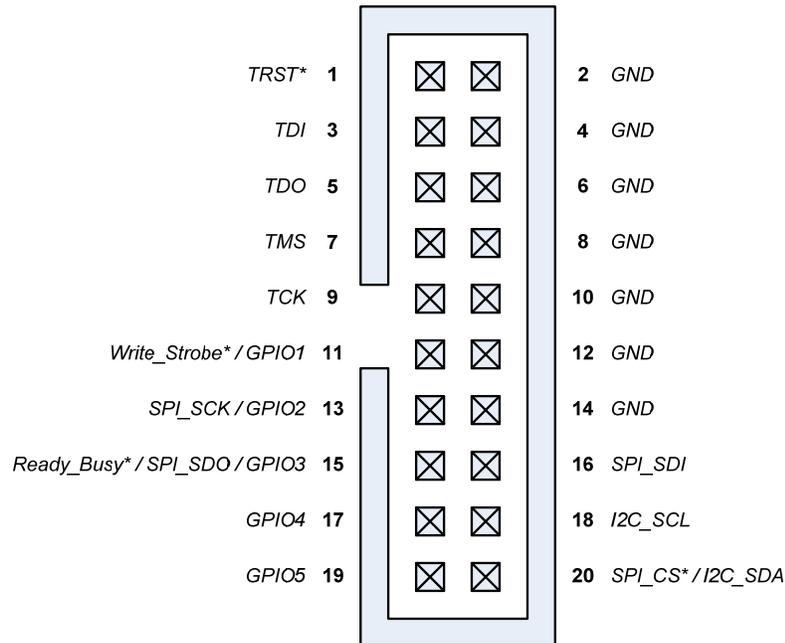


Figure A-5. Boundary-scan Flash Programming 20-Pin TAP Connector (top view)

Corelis' Flash Programming software supports the external signals Write_Strobe* and Ready/Busy*, in addition to the standard but slower scanned out/in signals approach.

The Write_Strobe* signal is active low and should be pulled up with a 1K resistor on the target board. It needs to be logically ORed with the flash Write-Enable (WE*) signal so that either the flash Write-Enable (WE*) signal or the external Write_Strobe* going low will assert the flash WE* input.

The active low Ready/Busy* signal is typically an open-collector/open-drain signal that ties directly to the same signal(s) on the Flash device(s). This enables multiple devices to drive it toward the USB-1149.1/1E.

Table A-5 summarizes the specifications for a 20-pin TAP connector without latch ejectors. Equivalent connectors are available from other manufacturers.

Reference	Description	Manufacturer	Part Number
Flash TAP	Straight header, 20-pin, 4 wall, with center notch	3M	2520-6002UG

Table A-5. Flash Programming TAP 20-Pin Connector

Table A-6 describes the signals:

Pin	Signal Name	Signal Description
1	TRST*	Test Reset (Input to the UUT)
2	GND	
3	TDI	Test Data In (Input to the UUT)
4	GND	
5	TDO	Test Data Out (Output from the UUT)
6	GND	
7	TMS	Test Mode Select (Input to the UUT)
8	GND	
9	TCK	Test Clock (Input to the UUT)
10	GND	
11	Write_Strobe* / SPI_CS2* / GPIO1	Discrete Output (Input to the UUT)
12	GND	
13	SPI_SCK / GPIO2	Discrete Output (Input to the UUT)
14	Reserved	[NOTE: may optionally be connected to GND]
15	Ready_Busy* / SPI_SDO (MISO) / GPIO3	Discrete Output (Input to the UUT)
16	SPI_SDI (MOSI)	Discrete Output (Input to the UUT) [NOTE: connect to GND if not used]
17	GPIO4	Discrete Output (Input to the UUT)
18	I2C_SCL	Discrete Output (Input to the UUT) [NOTE: connect to GND if not used]
19	GPIO5	Discrete Output (Input to the UUT)
20	SPI_CS1* / I2C_SDA	Discrete Output (Input to the UUT) [NOTE: connect to GND if not used]

Table A-6. USB-1149.1/1E 20-pin Target Connector Pin Assignment

Figure A-6 shows a typical schematic of the target TAP connector with termination resistors. The 1K pull-up resistors should connect to the target Vcc supply corresponding to the interface voltage (programmable on the USB-1149.1/1E from 1.25 to 3.3 V). Recommended resistor values are +/- 5%.

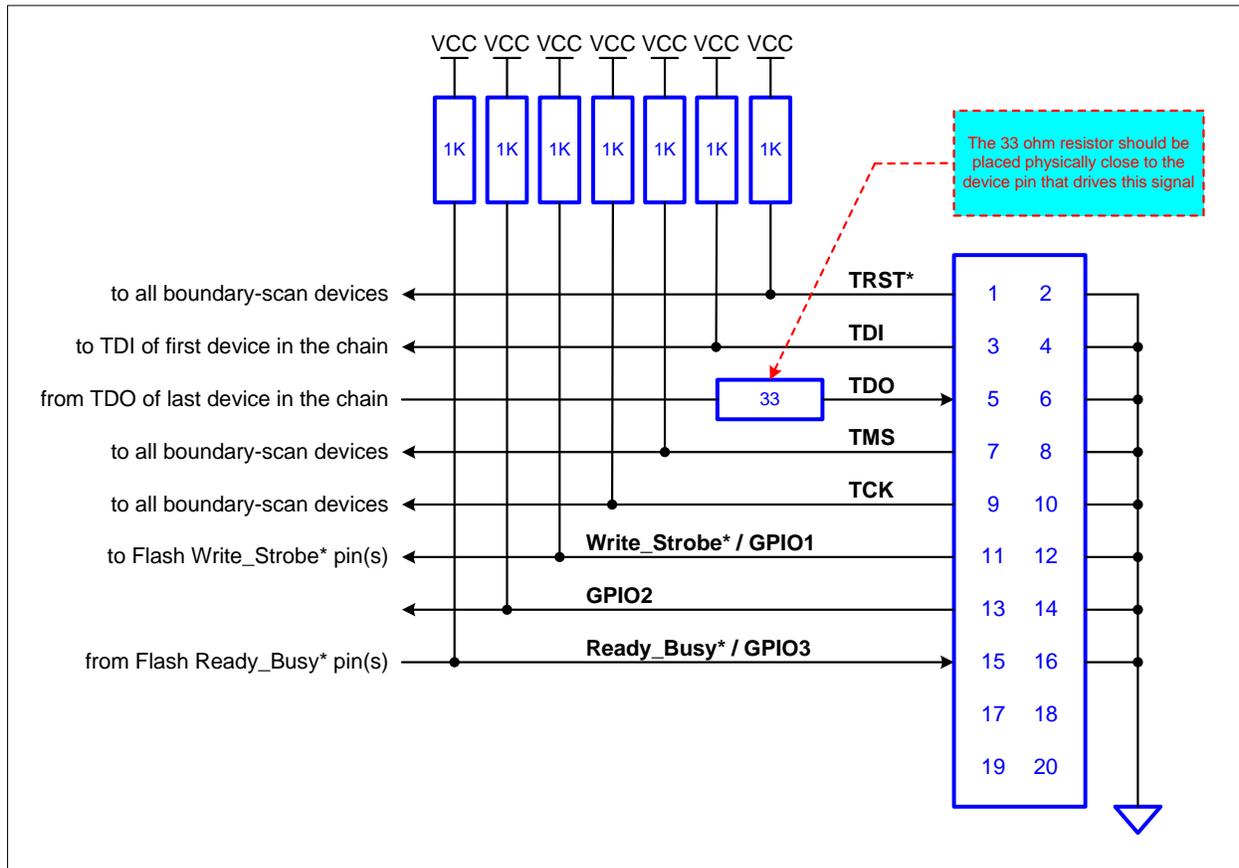


Figure A-6. 20-pin TAP Connector Schematic for JTAG

Figure A-7 shows the recommended 20-pin TAP connector schematic that supports JTAG and direct SPI programming.

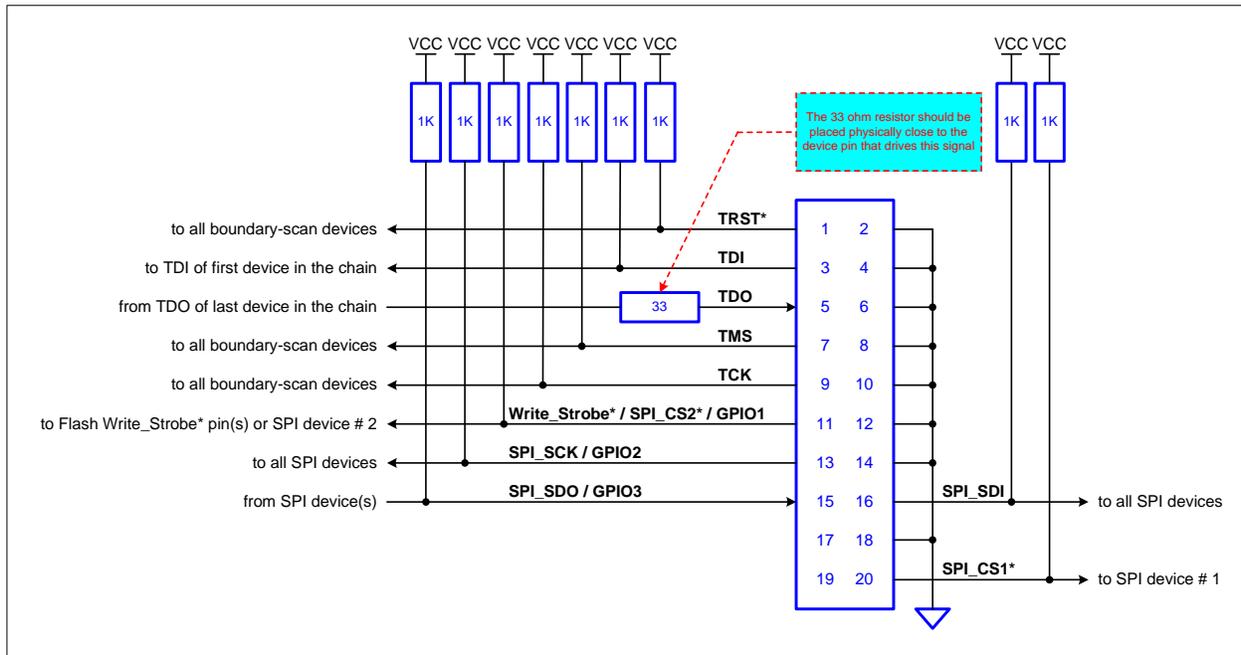


Figure A-7. 20-pin TAP Connector Schematic for Direct SPI Programming

Figure A-8 shows the recommended 20-pin TAP connector schematic that supports JTAG and direct I2C programming.

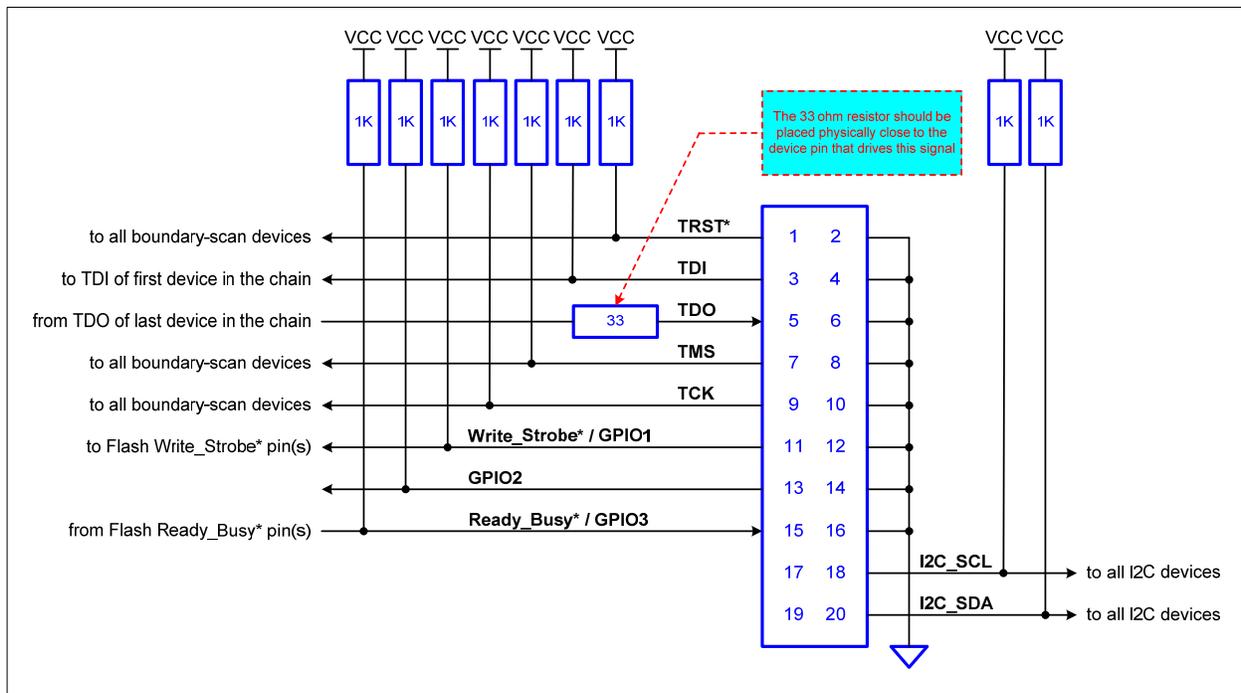


Figure A-8. 20-pin TAP Connector Schematic for Direct I2C Programming

Appendix B: Self Test Utility Software

The USB-1149.1/1E has a self test utility that can be used to test the unit and make sure that it is fully functional. Logic at the TAP connectors can read back data shifted out on TMS and TDO synchronously with the TCK. Using these signal paths, a host can test the TAP signals all the way to the connectors, verifying the overall functionality of the system.

Self-Test

The self-test utility is provided as an off-line confidence test only. Under normal circumstances there is no need to run the self-test utility software. However, if you suspect that the product is damaged, you can run the self-test on the USB-1149.1/1E module. The self-test utility is installed on your computer in the same folder where the ScanExpress Applications (ScanExpress Runner, ScanExpress Debugger and ScanExpress Programmer) applications are installed. Make sure to disconnect any target cables before running the test.

Using Windows Explorer, select and run the “**USB1149_1E_test.exe**” file. A small pop-up should appear. Click on **Test** to run the self-test.

The program should respond with results similar to the screen shown in Figure B-1.

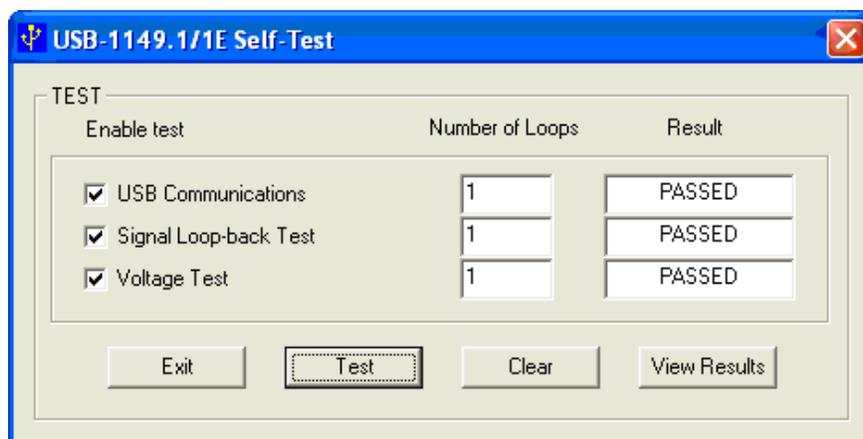


Figure B-1. Self-Test Results for the USB-1149.1/1E